Factsheet SI30USBSV10

Silicon Cores™

Core to the Intelligent System™

USB 2.0 VMM SystemVerilog VIP

Silicon Interfaces' USB 2.0 VMM SystemVerilog VIP is fully documented, off the shelf component for the verification of the USB 2.0 compliant Function Controller.

USB 2.0 VMM VIP is developed using the Synopsys VMM methodology that is used in dynamic simulation of USB 2.0 based design. Verification IP created according to the VMM methodology allows for easy "plug-and-play" use in VMM test benches.

The USB2.0 VIP uses SystemVerilog to create comprehensive verification environments using coverage-driven, constrained-random and assertion-based techniques. This VIP can work in a standalone mode i.e. can be plugged with any Function Controller with standard pinouts without disturbing the structure.

The VIP provides a fast and accurate way to simplify and speed-up the Device verification task. In a complex design process, verification may take up to 70% of the development time. USB 2.0 VMM SV VIP speeds up the verification process providing a compelling cost and time to market.

Silicon Interfaces' USB 2.0 function controller is a highly integrated solution for USB applications and provides 480 Mb/s high speed USB interface. It is a single core solution incorporating USB 2.0 protocol operating in Link Layer of Open System Interconnect (OSI) which significantly reduces the time and cost of implementing complex USB 2.0 target system designs.

Product Specifications

- The VIP can work with either 8-bit or 16-bit standard USB 2.0 Devices
- Error Injection Mechanism, which can be turned ON or OFF for a given simulation run incorporates around 45+ scenarios for different Error types
- Provides a choice of resetting the DUT to either High-Speed or Full-Speed Mode upon startup
- Supports RESET / SUSPEND / RESUME operation, as well as on-the-fly Reset switch- over from High-Speed to Full-Speed or vice-versa

Product Highlights

- ☑ Synopsys VMM complaint
- ☑ Absence of inter-module dependencies makes the VIP highly reusable
- ☑ Hierarchical Seed Randomization.
- ☑ Fully Constrained Driven Randomization of Packets achieved by Randomization of various fields of the Packet
- ☑ Intelligent and versatile Scoreboard that provides:
  - A bird's eye view of the USB Transactions
  - Total number of Transactions
  - Statistics of Transfer Types
  - Count of Token, Data and Handshake Packets sent / received
  - Statistics on RESET / SUSPEND / RESUME activities
  - Error Injection statistics
  - Overall count of good / bad Packets
- ☑ The following USB 2.0 Modes are supported:
  - Full-Speed / High-Speed 8-bit
  - Full-Speed / High-Speed 16-bit
  - Low-Speed Only
  - Full-Speed Only
- ☑ Programmable and Randomized Transfer Types, namely INTERRUPT, ISOCHRONOUS, BULK and CONTROL
- ☑ Provides a choice for inhibiting SUSPEND and / or RESET operation through use of simple macros
- ☑ Auto Programming – cum selection of Clocks for different Modes – 6 MHz (Low-Speed Only Mode), 30 MHz (16-bit High-Speed / Full-Speed Mode), 48 MHz (Full-Speed Only Mode) or 60 MHz (8-bit High-Speed / Full-Speed Mode)
- ☑ Supports up to 16 Endpoints as per the USB 2.0 Standard. Endpoints can be either IN, OUT or NOT_IMPLEMENTED through user-defined header declarations, with Endpoint0 as INOUT

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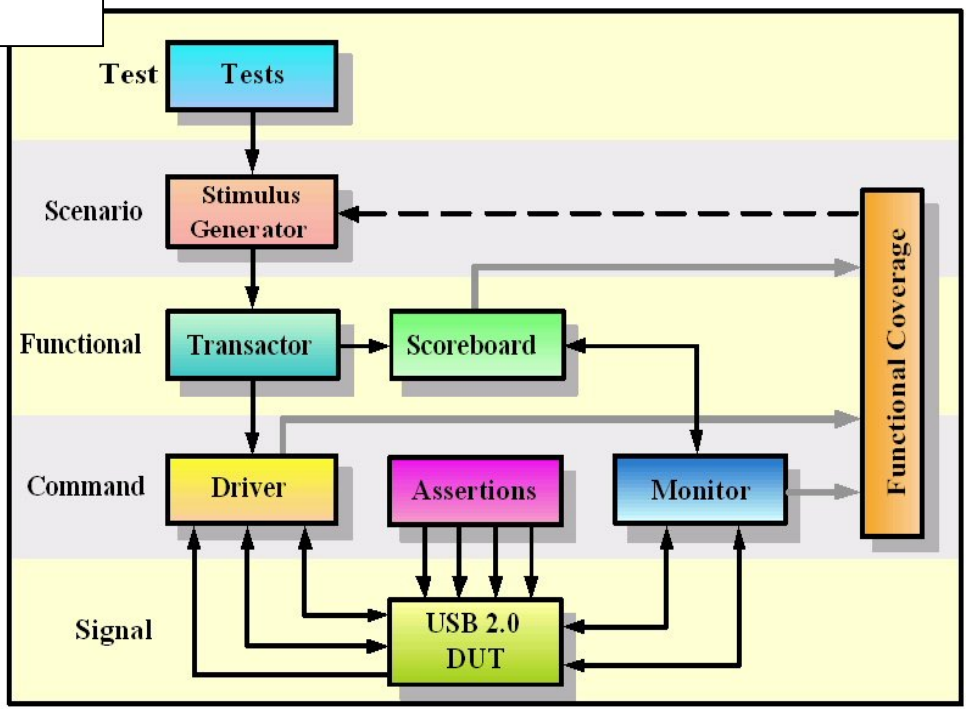
USB 2.0 VMM Test Environment



Layered Testbench Architecture:

The Layered Testbench architecture is a key aspect of a reusable design as shown in the following figure .It provides abstraction at different levels and easy Plug-n-Play along with concurrent development of various verification environment pieces.

Test Layer: Test Layer provides additional testcase-specific self-checking not provided by the Functional Layer at the Transaction Level. It can also perform checks where correctness depends on timing with respect to a particular Synchronization Event introduced by the testcase.

Command Layer: The Command Layer typically contains Bus-Functional Models, Physical-Level Drivers and Monitors associated with the various Interfaces and Physical-Level Protocols present in the DUT. It provides a consistent, Low-Level Transaction Interface to the DUT, regardless of how the DUT is modeled.

Functional Layer: The Functional Layer provides the necessary Abstraction Layers to process Application-Level Transactions and verify the correctness of the DUT.

Signal Layer: This layer provides Signal-Level Connectivity in the physical representation of the DUT. This layer provides Signal Name Abstraction and connectivity to the event driven world of most simulation engines. This layer chiefly comprises the BFM module.

VMM ENVIRONMENT BLOCK DIAGRAM DESCRIPTION

Stimulus Generator: This generates the Stimulus Packets. These Packets are constraint driven randomized raw data that is passed to the Transactor.
Transactor / BFM: It determines the sequence of the Packets and also the type of Packet to be sent to the Driver.
Driver: A Driver converts the transactions into appropriate signal-level activity as per the design specifications.
Monitor: It extracts the transactions from the observed interface and puts that newly assembled transactions onto a channel.
Scoreboard: It receives information from the Transactor as well as from the monitor, based on this information; it keeps a count of the types of Transaction and the various attributes of the Transactions.
Functional Coverage: It measures how much of the original design specification have been exercised.
DUT: The Device under Test.

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